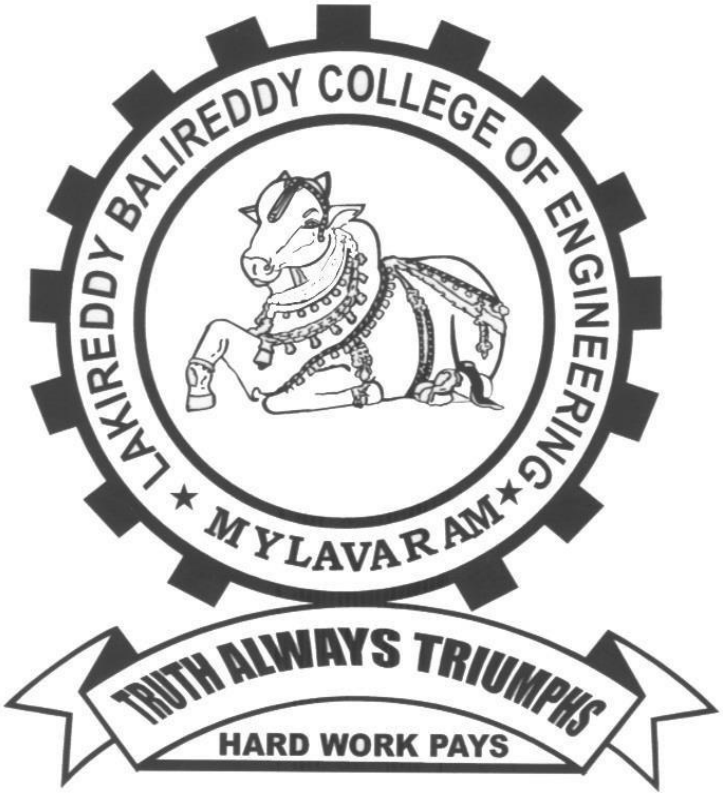
ELECTRICAL & ELECTRONICS ENGINEERING WORKSHOP



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BASIC ELECTRICAL & ELECTRONICS ENGINEERING WORKSHOP

Name :

Regd.No :

Course :

Branch :

Academic Year :

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ELECTRICAL&ELECTRONICSENGINEERINGWORKSHOP

(Common to All branches of Engineering)

Coursecode:23EE51
Course Title: Basic Electrical & Electronics Engineering Workshop.
Regulation : R23

Course Objectives:

To impart knowledge on the fundamental laws & theorems of electrical circuits, functions of electrical machines and energy calculations.

Course Outcomes:

After competition of this course, the student will be able to

CO1.Compute voltage, current and power in an electrical circuit.**(Apply)**
CO2.Computemedium resistance using Wheatstone bridge.**(Apply)**
CO3.Discovercriticalfieldresistance and critical speed of DC shunt generators.**(Apply)**
CO4.Estimatereactivepowerandpower factor in electrical loads.**(Understand)**
CO5: Plot the characteristics of semiconductor devices.**(Apply)**
CO6: Demonstrate the working of various logic gates using ICs.**(Understand)**

BASIC ELECTRONICS ENGINEERING

Course Objectives:

- To teach the fundamentals of semiconductor devices and its applications, principles of digital electronics.

Course Outcomes: After the completion of the course students will be able to

CO1: Interpret the characteristics of various semiconductor devices **(Knowledge)**
CO2: Infer the operation of rectifiers, amplifiers.**(Understand)**
CO3: Contrast various logic gates, sequential and combinational logic circuits.**(Understand)**

INDEX

S.No	Date	Name of the Experiment	Marks	Signature
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				
10.				
11.				
12.				
13.				
14.				

PLOT V-I CHARACTERISTICS OF PN JUNCTION DIODE A) FORWARD BIAS B) REVERSE BIAS.	EXPT NO: 1
	DATE:

AIM: 1. To Plot the V-I characteristics of PN junction diode.

2. To find the resistances in Forward and Reverse Bias mode.

APPARATUS REQUIRED:

1. IN 4007 Diode	1.No.
2. Resistor 1KΩ	1.No.
3. 0-50mA DC Ammeter	1.No.
4. 0-500 μ A DC Ammeter	1.No.
5. 0-1V Dc Voltmeter.	1.No.
6. 0-30V DC Voltmeter	1.No.
7. 0-30V Regulated Power Supply	1.No.
8. Bread Board	1.No.

THEORY:

Forward Bias:

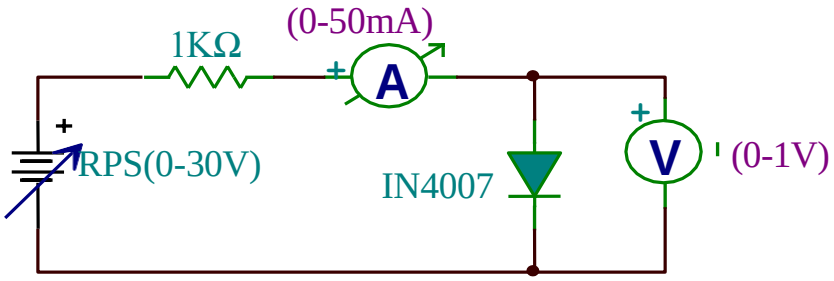
If P-type semiconductor is connected to the positive terminal of the battery and N-type Semiconductor is connected to negative terminal of the battery, this way of biasing is called as forward bias. In this biasing current is exponentially increasing with respective to applied voltage.

Reverse bias:

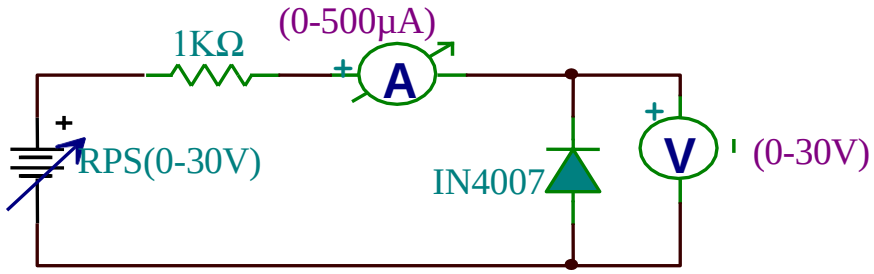
If P-type semiconductor connected to negative terminal of the battery and N-type semiconductor is connected to the positive terminal of the battery is known as reverse bias. In reverse bias the current through the diode is I = -Io whose value is independent on applied voltages and which depends on minority carrier concentration and temperature. For every 10 degrees raise in temperature reverse saturation current becomes double.

Thus in forward bias diode offers less resistance and in reverse bias diode offers high resistance.

CIRCUIT DIAGRAMS:



FORWARD BIAS CHARACTERISTICS



REVERSE BIAS CHARACTERISTICS

PROCEDURE:

FORWARD BIAS CHARACTERISTICS:

1. Connect the Circuit as per the Circuit Diagram on the bread board.
2. Use DMM for voltage Measurement.
3. Switch on the regulated Power supply and slowly increase the source voltage and note the down the voltage across the PN Junction diode insteps of 0 .1Volt and note down the Corresponding diode current under forward bias Condition as per table given below.
4. Plot the graph V_f versus I_f on the graph Sheet.
5. From the graph find out the forward bias resistance of the diode
6. Observe and note down the cut in Voltage of the diode.

$R = V_f/I_f$.

TABLE:

FORWARD BIAS CHARACTERISTICS:

S.No	FORWARD BIAS VOLTAGE (V_f) IN VOLTS	FORWARD BIAS CURRENT (I_f) IN mA
1		
2		
3.		
4.		
5.		
6.		
7.		
8.		
9		
10		
11		
12		

REVESE BIAS CHARACTERISTICS:

1. Connect the Circuit as per the Circuit Diagram on the bread board.
2. Switch on the Regulated Power supply and slowly increase the source Voltage and note the Voltage across the PN Junction diode insteps of 1 Volt. And note the Corresponding current flowing through the diode under reverse bias Condition as per table given below.
3. Plot the graph V_r versus I_r on the graph Sheet.
4. From the graph find out the reverse bias resistance of the diode

   $R = V_r/I_r$.

REVERSE BIAS CHARACTERISTICS:

S.No	REVERSE BIAS VOLTAGE (V_r) IN VOLTS	REVERSE BIAS CURRENT (I_r) IN μA
1		
2		
3.		
4.		
5.		
6.		
7.		
8		
9		
10		
11		
12		
13		
14		
15		

MODEL GRAPH:

PRECAUTIONS:

1. Identify the Diode terminals properly while connecting.
2. Keep all COARSE controls of RPS minimum and CURRENT controls in maximum position before switch ON.

RESULT:

1. Cut in voltage =
2. Forward resistance =
3. Reverse resistance =

The V-I Characteristics of the PN Junction diode are plotted for the Both forward and reverse bias conditions and Calculated the forward and reverse bias resistance.

VIVA QUESTIONS:

1. What is meant by P- type layer?
2. What is meant by N- type layer?
3. What is the function of p-n junction diode?
4. What is meant by forward bias of p-n junction diode?
5. What is meant by reverse bias of p-n junction diode?
6. Define cut-in voltage of p-n junction diode.
7. What is meant by depletion layer in p-n junction diode?

Plot V – I characteristics of Zener Diode and its application as voltage Regulator	EXPT. NO: 2
	DATE:

AI M: - 1. To Plot the V-I characteristics of ZENER diode.

2. To find out the Zener Break down Voltage and Zener resistances from the Characteristics and observe the use of zener diode as voltage regulator in reverse bias mode.

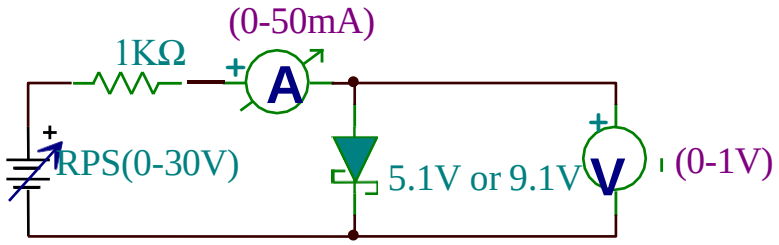
APPARATUS REQUIRED:-

1. D.C Regulated Power Supply 0-30V	1No.
2.Zener Diodes	1No.
3.Resistor 1 KΩ	1No.
4.DC Ammeter 0-50mA	2No.
5.DC Voltmeters 0-1V,0-30V Each	1No.
6. Bread Board.	1No.

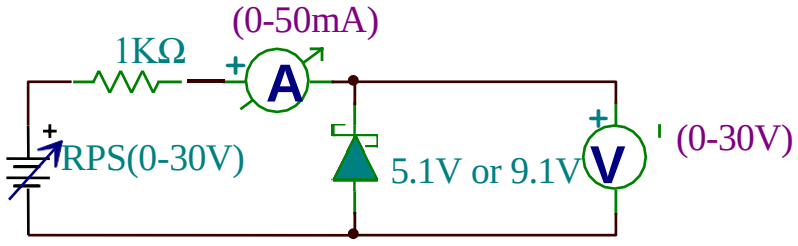
THEORY:

In forward bias it acts as similar to the diode. In the reverse bias it acts as regulator because its doping concentration is higher than the ordinary diode, due to this a large electric field intensity is developed at the junction with narrow distance. Thus a large amount of current is drawn through the diode. This phenomenon is known as Zener Break. The diode which adopts this is zener diode.

CIRCUIT DIAGRAMS:-



FORWARD BIAS CHARACTERISTICS



REVERSE BIAS CHARACTERISTICS

PROCEDURE:-

Forward bias characteristics:-

1. Connect the Circuit on the Bread Board as per the Circuit Diagram given below.
2. Switch on the D.C regulated power supply and slowly increase the source Voltage and note the Voltage across the Zener diode in steps of 0.1V and note thecorresponding diode current under forward bias condition as per the tabular form given below.
3. Draw graph between voltage across the diode (V_f) Versus current (I_f) through thediode on graph sheet for both zener diodes.

Reverse bias characteristics:-

1. Connect the circuit on the Bread Board as per the Circuit Diagram given above.
2. Switch the DC Regulated power supply and slowly increase the source Voltage and note down the Voltage across Zener diode insteps of the 1Volt and note the Corresponding diode current as per table given below.
3. Draw the graph between Voltage across the Zener diode (V_r) Versus current (I_r) through the diode on graph sheet;
4. From the graph find out the Zener break down voltage& Zener resistance.

$$Z\,r = \frac{V_r}{I_r}.$$

TABULAR FORMS:-

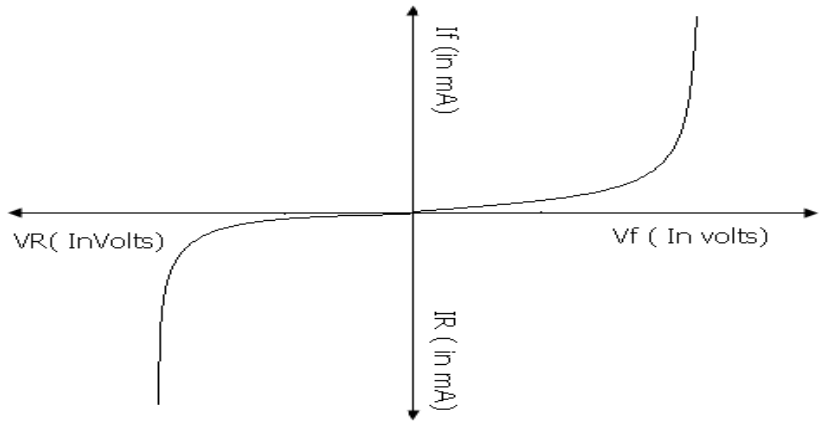
FORWARD BIAS CHARACTERISTICS:-

S.No	Forward Voltage(V_f)in Volts	Forward Current(I_f) in mA

REVERSE BIAS CHARACTERISTICS:-

S.No.	Reverse Voltage(V_r) In Volts	Reverse Current(Ir) inmA

MODEL GRAPH:-



PRECAUTIONS:

1. Identify the Diode terminals properly while connecting.
2. Keep all COARSE controls of RPS minimum and CURRENT controls in maximum position before switch ON.

RESULT: **1.** Zener Break down Voltage =

2. Zener resistance =

The Characteristics of the Forward and Reverse biased Zener Diode and the Zener Break down Voltage from the Characteristics are Observed.

VIVA QUESTIONS:

1. What is meant by Avalanche effect?
2. What is meant by Zener effect?
3. What is doping concentration of zener diode?
4. What is meant by Zener break down voltage?

Implementation of Half wave rectifier	EXPT. NO: 3(a)
	DATE:

AIM: To observe the input & output waveforms of Half-Wave Rectifier with and without filter. And to find the Ripple factor & Percentage of load Regulation.

APPARATUS:

1. Transformer 230v/6v – 0 – 6v -1No
2. Diodes IN4007 -1 No
3. Decade resistance Box -1 No
4. Multi meter -1 No
5. Bread Board -1 No
6. 20MHz Dual Trace CRO -1 No
7. Connecting wires

THEORY:

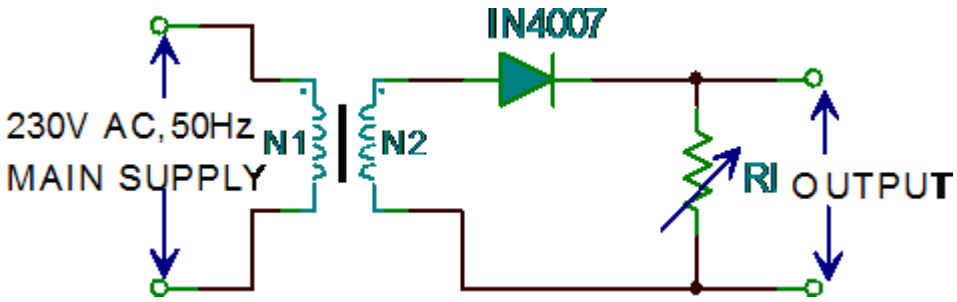
As per the circuit diagram, it contains transformer and one diode, DRB, Capacitor. During the positive swing of power supply, the diode acts as forward bias condition. Hence it offers very less resistance. Thus whatever the input signal is applied transmitted to the load resistance when the negative swing of the A.C signal is applied to the diode, it acts as reverse bias connection Since it offers as high resistance. In this no signal is allowed to the load. Thus it gives Half wave output signal .The amount of A.C signal is present in output wave form is measured by ripple factor.

$$\text{Ripple factor} = \frac{V_{rms}}{V_{dc}}$$

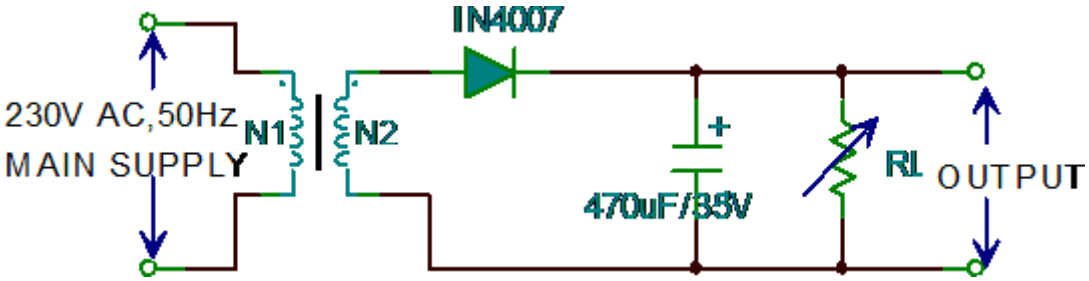
$$\text{Percentage of Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

CIRCUIT DIAGRAMS:-

HALF WAVE WITHOUT FILTER



HALF WAVE WITH FILTER



PROCEDURE:

1. Connecting the circuit on bread board as per the circuit diagram
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the RL value to 500Ω
4. connect the Multi meter at output terminals and vary the load resistance (DRB) from500Ω to 5KΩ and note down the Vac and Vdc as per given tabular form
5. Disconnect load resistance (DRB) and note down No load voltage Vdc.
6. Connect load resistance at 5KΩ and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet
7. Calculate Ripple Factor $\gamma = \frac{V_{ac}}{V_{dc}}$
8. Calculate Percentage of regulation = $\frac{V_{noload} - V_{full\ load}}{V_{full\ load}} \times 100\%$

TABULAR FORM: Without filter

V no Load Voltage (V_{dc}) =

S.NO	Load Resistance In Ohms	Vdc (Volts	Vac (Volts)	Ripple Factor γ	%of Regulation $\frac{V_{NL} - V_{FL}}{V_{FL}}$ X 100
1	500				
2	5K				

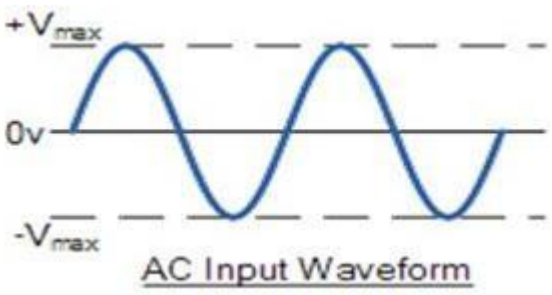
TABULAR FORM: With filter

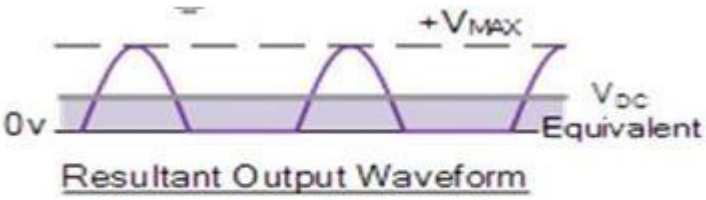
V no Load Voltage (V_{dc}) =

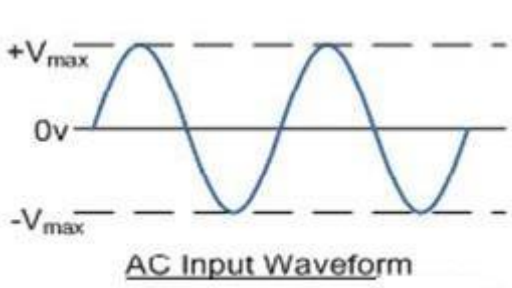
S.NO	Load Resistance In Ohms	Vdc(Volts)	Vac (Volts)	Ripple Factor γ	%of Regulation $\frac{V_{NL} - V_{FL}}{V_{FL}}$ X100
1	500				
2	5K				

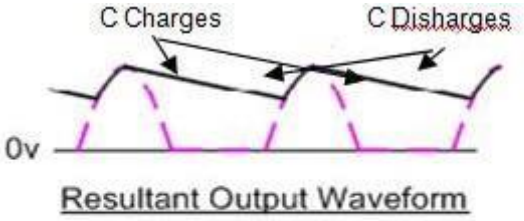
WAVE SHAPES:

HALF WAVE WITHOUT FILTER









HALF WAVE WITH CAPACITIVE FILTER

PRECAUTIONS:

1. Don't touch the Primary side of the Transformer when it is PLUG-IN.
2. Maintain R_L(DRB) should be above 100 Ω.

RESULTS: Average Ripple factor without filter =

Average Ripple factor with filter=

Average Percentage of load Regulation without filter=

Average Percentage of load Regulation with filter =

Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Half wave rectifiers with & without filter.

VIVA QUESTIONS:

1. What is the function of half wave rectifier (HWR)?
2. What is meant by voltage regulation of HWR?
3. What are the applications of HWR?
4. What is the value of peak inverse voltage of HWR?
5. What is the value of ripple factor in HWR?

Implementation of Full wave rectifier	EXPT. NO: 3(b)
	DATE:

AIM: To observe the input & output waveforms of Full- Wave Rectifier with and without filters. And to find the Ripple factor and Percentage of load Regulation.

APPARATUS:

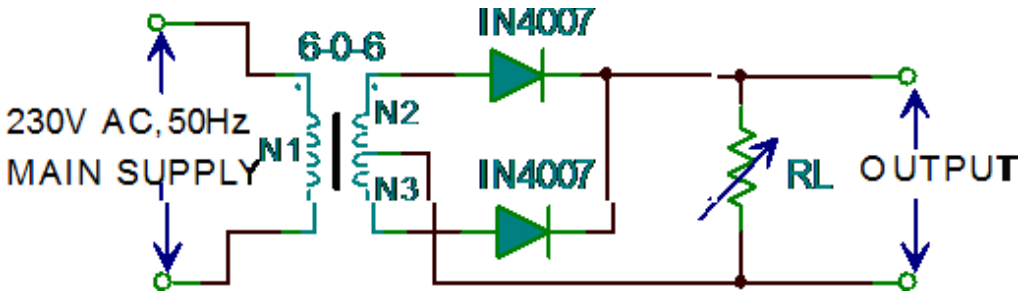
1. Transformer 230v/6v – 0 – 6v - 1 No
2. Diodes IN4007 - 2 Nos
3. Capacitor 470µf/35v - 1 No.
4. Decade resistance Box -1No
5. Multi meter -1No
6. Bread Board -1 No
7. 20MHz Dual Trace CRO -1 No

THEORY:

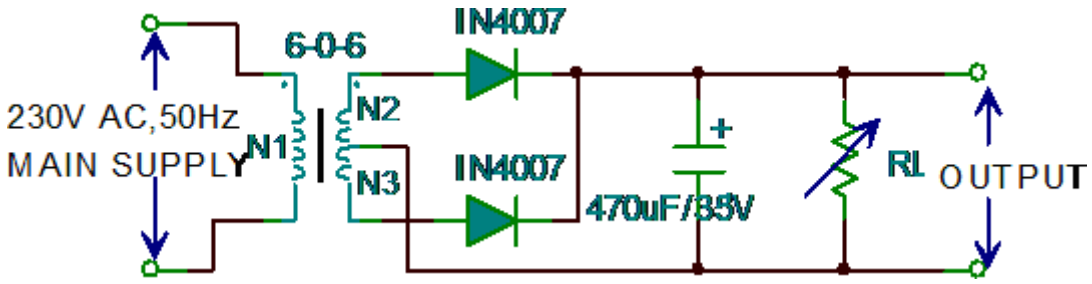
It contains two diodes connected across the load and a center tapped transformer. When the input is 0 to Π due to the center tapping we have two waveforms which are in opposite phase. Diode1 acts as a conductor in 0 to Π. The diode 2 acts as a non-conductor. Hence the output is almost equal to input of diode 1.When the primary of transformer is between Π to 2Π diode 1 acts as non-conductor and diode 2 acts as conductor. Hence the output signal is almost equal to input signal of diode2 Thus we can observe a continuous waveform.

CIRCUIT DIAGRAM:

FULL WAVE WITHOUT FILTER



FULL WAVE WITH FILTER



PROCEDURE:

1. Connecting the circuit on bread board as per the circuit diagram
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the RL value to 100Ω
4. Connect the multi meter at output terminals and vary the load resistance (DRB) from100Ω to 5KΩ and note down the V_{ac} and V_{dc} as per given tabular form
5. Disconnect load resistance (DRB) and note down No load voltage Vdc
6. Connect load resistance at 1KΩ and connect CH – I of Dual Trace CRO at Secondary (Input) terminals, Channel – II of Dual Trace CRO at output terminals and observe and note down the Input and Output Wave form on Graph Sheet
7. Calculate Ripple Factor $\gamma = \frac{V_{ac}}{V_{dc}}$
8. Calculate Percentage of regulation = $\frac{V_{noload} - V_{full\ load}}{V_{full\ load}} \times 100\%$

TABULAR FORM: Without filter

V no Load Voltage (V_{dc}) =

S.NO	Load Resistance In Ohms(RL)	V_{dc} (Volts	V_{ac} (Volts)	Ripple Factor γ	%of Regulation $\frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$
1					
2					

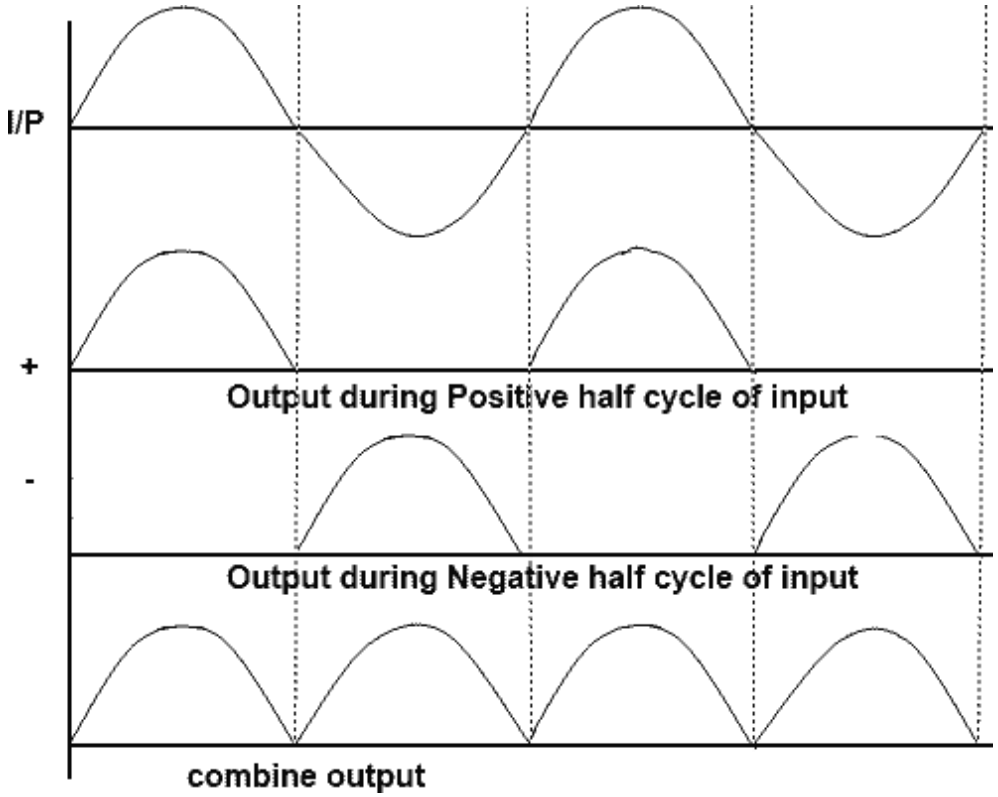
TABULAR FORM: With filter

V no Load Voltage (V_{dc}) =

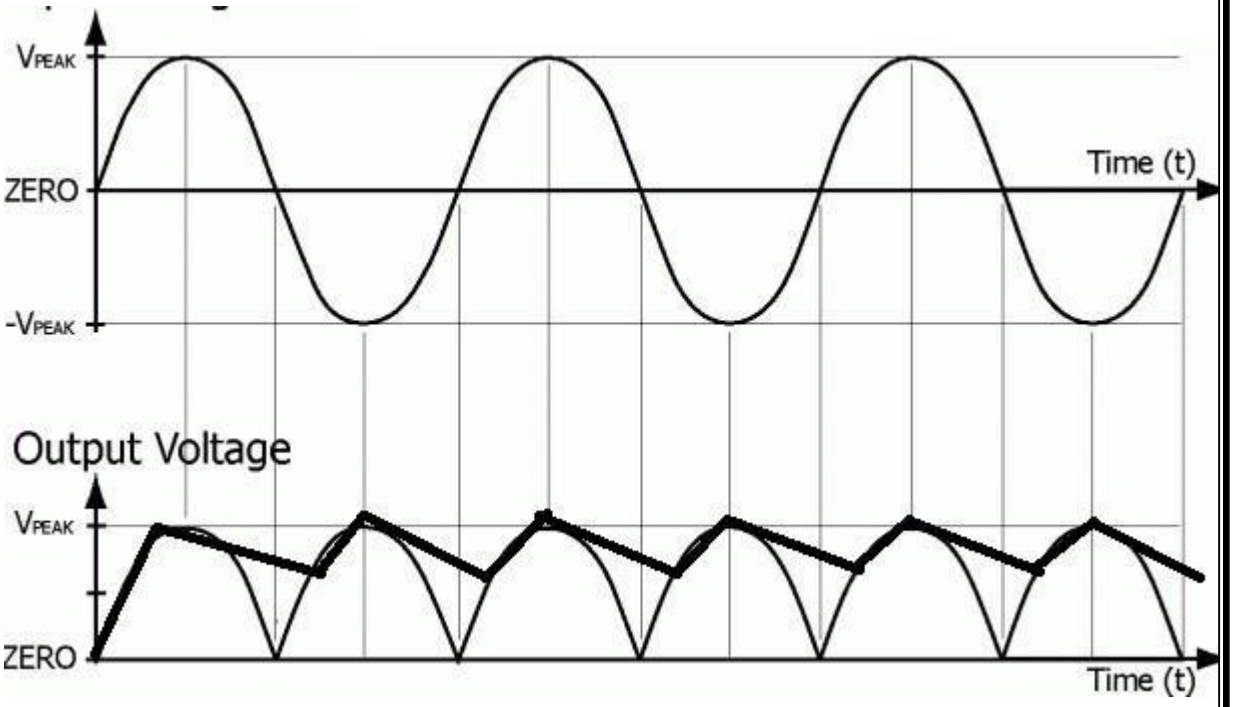
S.No	Load Resistance In Ohms	V_{dc} (Volts)	V_{ac} (Volts)	Ripple Factor γ	%of Regulation $\frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$
1	1K				
2	2K				

WAVE SHAPES:

FULL WAVE WITHOUT FILTER



FULL WAVE WITH FILTER



PRECAUTIONS:

1. Don't touch the Primary side of the Transformer when it is PLUG-IN.
2. Maintain R_L(DRB) should be above 100 Ω.

RESULTS: Average Ripple factor without filter =

Average Ripple factor with filter =

Average Regulation without filter =

Average Regulation with filter =

Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Full wave wave rectifiers with & without filter

VIVA QUESTIONS:

1. What is the function of full-wave rectifier (FWR)?
2. What is meant by voltage regulation of FWR?
3. What are the applications of FWR?
4. What is the value of peak inverse voltage of FWR?
5. What is the value of ripple factor in FWR?

Plot Input and Output Characteristics of BJT in Common Base Configuration	EXPT NO: 4(a)
	DATE:

AIM: To Plot input and output Characteristics of BJT in Common Base Configuration and find input and output resistances.

APPARATUS:

1. Transistor BC 107 or SL 100	1No.
2. Resistor 1KΩ	1No.
3. Ammeter 0-50mA	2No.
4. Voltmeter 0-1V, 0-30V	2No.
5. 0-30V, 1A Dual Channel power supplies	1No.
6. Bread Board,	1No.
7. Connecting wires	

THEORY:

In a common Base transistor base terminal is connected common to both the input (Emitter – Base) voltage and the output (collector –base) voltage. Voltmeters and Ammeters are connected to measure the input and output voltages and currents.

Input Characteristics:

To determine the input characteristics, the output (Collector-Base) Voltage is maintained constant, and the input (Emitter-Base) voltage is set at several convenient levels. For each level of the input voltage, the input current (Emitter current) is recorded.

(a) **Input Resistance (R_i)** :

The Emitter current increases rapidly with small increase in V_{BE} . This means that input resistance is small. It is defined by the ratio of V_{BE} to change in I_E at constant V_{CB}.

$$R_i = \frac{V_{BE}}{I_E} \quad \text{at constant } V_{CB}$$

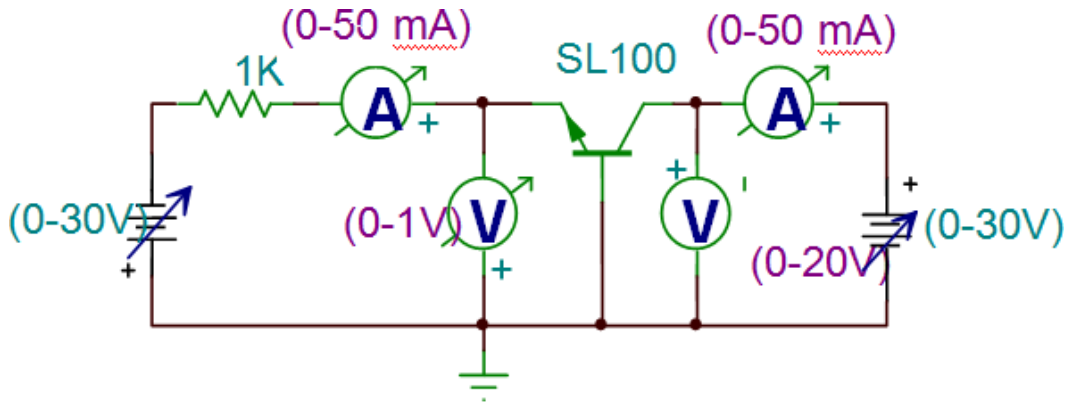
Output Characteristics:

To determine the output characteristics the input (Emitter) Current is held constant at each of several fixed levels. For each fixed level of I_E, the output voltage V_{CB} is adjusted in convenient steps, and the corresponding levels of collector current are recorded.

Output resistance (R_O): It is the ratio of change in output voltage to corresponding change in output current at constant V_{CB}.

$$R_O = \frac{V_{CB}}{I_C} \quad \text{at constant } I_E$$

CIRCUIT DIAGRAM:



COMMON BASE TRANSISTOR CHARACTERISTICS

PROCEDURE:

Input characteristics:

1. Connect the circuit as in the circuit Diagram.
2. Make V_{CB} open and vary the 30V Supply (Channel-1) and note the Values of I_E and V_{BE}.
3. Adjust V_{CB} = 1V (Channel -2) Power supply.
4. Vary the 0-30V (Channel -1) power Supply and note the Values of I_E and V_{BE}.
5. Calculate Input resistance $R_i = \frac{V_{BE}}{I_E}$ **at constant V_{CB}**

TABULAR FORM:-

S.No	V_{CB}=open(0V)		V_{CB} = 1V	
	V_{BE}(V)	I_E(mA)	V_{BE}(V)	I_E(mA)

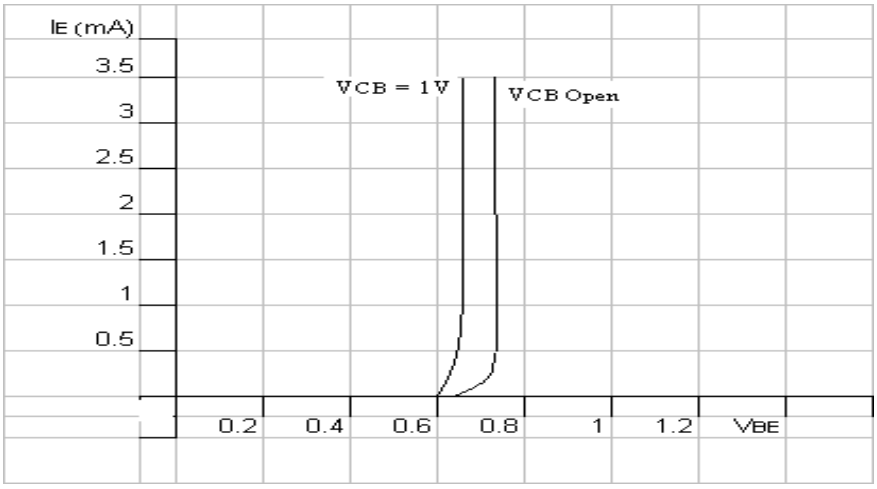
Output characteristics:-

1. Connect the circuit as shown in circuit Diagram.
2. Adjust the 0 – 30V (Channel – 1) power supply and fix the I_E=1mA value.
3. Vary the 0 – 30 V (Channel – 2) power supply and note the value of I_c *and* V_{CB}
4. Vary the V_{CB} in the order of 1V.
5. Repeat steps 2 to 4 for I_E = 1.5mA
6. Calculate output resistance $R_o = \frac{V_{CB}}{I_C}$ **at constant I_E**

TABULAR FORM:-

S.No.	I_E=1mA		I_E=1.5mA	
	V_{CB}(v)	I_C(mA)	V_{CB}(v)	I_C(mA)

GRAPH:-



INPUT CHARACTERISTICS

OUTPUT CHARACTERISTICS

1. Plot the input characteristics by taking I_E on y – axis and V_{BE} on X – axis
2. Plot the output characteristics by taking I_c on y – axis and V_{CB} on X – axis

PRECAUTIONS:

1. Keep all COARSE controls of RPS minimum and CURRENT controls in maximum position before switch ON.
2. Carefully connect the transistor terminals.

RESULT:

Input resistance R_i =
Output resistance R_o =

Input and output characteristics of CB Transistor are plotted.

VIVA QUESTIONS:

1. Explain early effect in CB configuration?
2. Give the relation between I_B and I_C .
3. Define large signal current gain.
4. Define emitter efficiency.

Plot Input and Output Characteristics of BJT in Common Emitter Configuration	EXPT NO: 4(b)
	DATE:

AIM: To Plot input and output Characteristics of BJT in Common Emitter Configuration and find input and output resistances.

APPARATUS:

1. Transistor BC 107 or SL 100	1No.
2. Resistor 1KΩ	1No.
3. Ammeter 0-50mA, 0-500μA	2No.
4. Voltmeter 0-1V, 0-30V	2No.
5. 0-30V,1A Dual Channel power supply	1No.
6. Bread Board	1No.
7. Connecting wires	

THEORY:

In a common Emitter transistor Emitter terminal is connected common to both the input (Emitter – Base) voltage and the output (Collector – Emitter) voltage. Voltmeters and Ammeters are connected to measure the input and output voltages and currents.

Input Characteristics:

To determine the input characteristics, the output (Collector- Emitter) Voltage is maintained constant, and the input (Emitter-Base) voltage is set at several convenient levels. For each level of the input voltage, the input current (Base-current) is recorded.

(b) **Input Resistance (R_i)** :

The Base current increases rapidly with small increase in V_{BE} . This means that input resistance is small. It is defined by the ratio of V_{BE} to change in I_B at constant V_{CE}.

$$R_i = \frac{V_{BE}}{I_B} \quad \text{at constant } V_{CE}$$

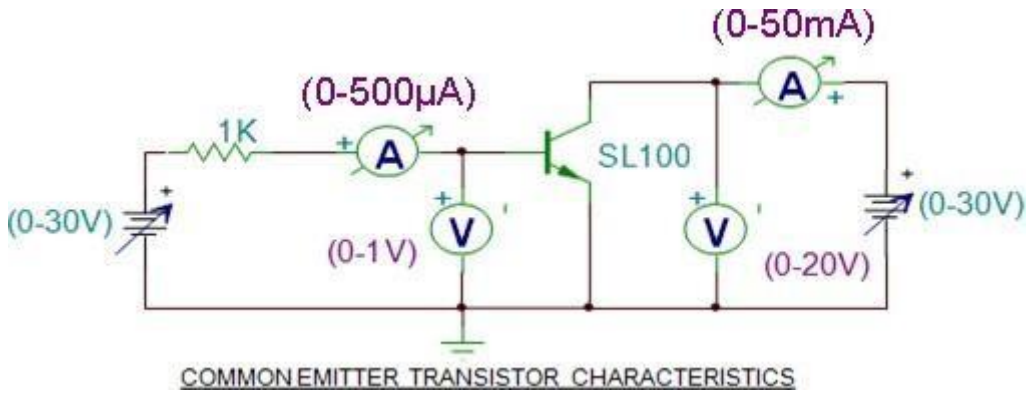
Output Characteristics:

To determine the output characteristics the input (Base) Current is held constant at each of several fixed levels. For each fixed level of I_B, the output voltage V_{CE} is adjusted in convenient steps, and the corresponding levels of collector current are recorded.

(b) **Output resistance (R_O) :** It is the ratio of change in output voltage to corresponding change in output current at constant V_{CB}.

$$R_O = \frac{V_{CE}}{I_C} \quad \text{at constant } I_B$$

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the Circuit as shown in the Circuit Diagram.
2. Make V_{CE} Open and Vary the 30 V Supply (Channel 1) and note the Values of I_B and V_{BE}.
3. Adjust V_{CE} = 1V in Channel 2 Power supply.
4. Vary the 0-30V (Channel 1) power Supply and note the Values of I_B and V_{BE}

5Calculate Input resistance $R_i = \frac{V_{BE}}{I_B}$ **at constant V_{CE}**

TABULAR FORM:

S.No.	V_{CE}= 0 V Open		V_{CE} = 1V	
	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)

OUTPUT CHARACTERISTICS:

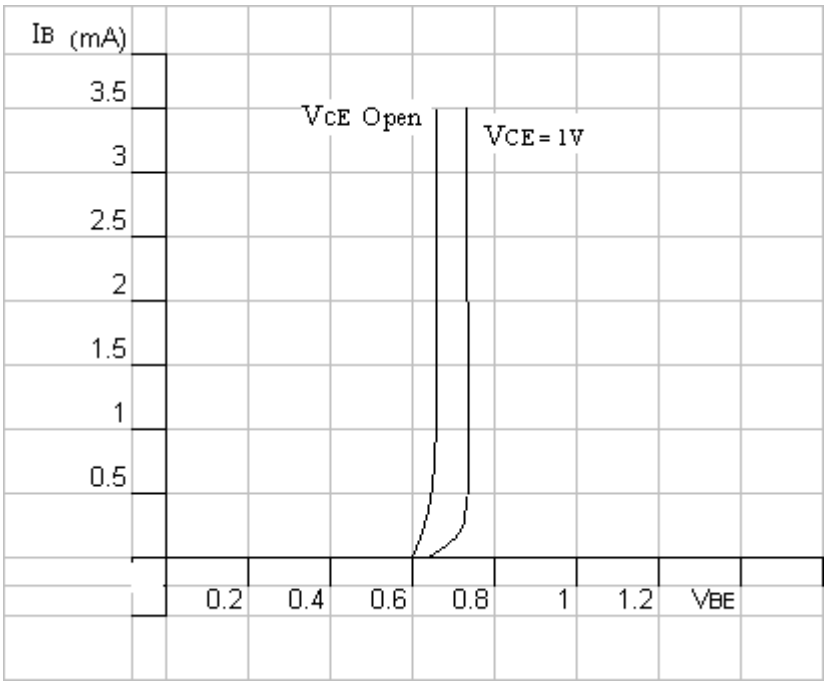
1. Connect the Circuit as shown in the Circuit Diagram.
2. Connect 0-500 μ A Ammeter in place of 0-50mA.
3. Adjust 0-30V (Channel -1) power Supply and fix the Values of I_B = 100 μ A
4. Vary the V_{CE} 0-30V (Channel -2) power supply and note down the Values of the Ic and V_{CE}. Vary in the Steps of 1V.
5. Repeat the steps 3 & 4 for I_B = 200 μA
6. Calculate Input resistance $R_o = \frac{V_{BE}}{I_C}$ at constant I_B

TABULAR FORM:

S.No.	I_B = 100 μA		I_B = 200 μA	
	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_C(mA)

GRAPH :

1. Plot the input characteristics by taking I_B on Y-Axis and V_{BE} on X-Axis.
2. Plot the output characteristics by taking I_C on the Y-Axis and V_{CE} on X - Axis



INPUT CHARACTERISTICS

OUTPUT CHARACTERISTICS

PRECAUTIONS:

1. Keep all COARSE controls of RPS minimum and CURRENT controls in maximum position before switch ON.
2. Carefully connect the transistor terminals.

RESULT: Input resistance R_i =

Output resistance R_o =

Input and output characteristics of CE Transistor are plotted.

VIVA QUESTIONS:

1. Give the relation between I_B, I_C and I_E
2. Give the relation between I_{CEO} and I_{CBO}.
3. Define the transport factor.
4. Define saturation region, cut-off region and active region.

Verification of Truth Table of AND, OR, NOT, NAND, NOR, EX-OR Using Integrated Circuits	EXPT NO: 5
	DATE:

AIM:

To study of logic gates and verify their truth tables using IC's.

APPARATUS REQUIRED:

i) IC 7408, IC7432, IC7404

ii) LEDs

iii) Breadboard

iv) Connecting Wires

THEORY:

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output. OR, AND, NOT are basic gates.

i) AND GATE:(IC7408)

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

ii) OR GATE: (IC7432)

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low-level when both the inputs are low.

iii) NOT GATE:(IC7404**)**

The NOT gate is called an inverter. The output is high when the input is low.

The output is low when the input is high.

iv) NAND GATE: (IC7400)

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low. The output is low level when both inputs are high.

v) NOR GATE:(IC7402**)**

The NOR gate is a contraction of OR-NOT.

The output is high when both inputs are low. The output is low when one or both inputs are high.

vi) Ex-ORGATE: (IC7486)

The output is high when anyone of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

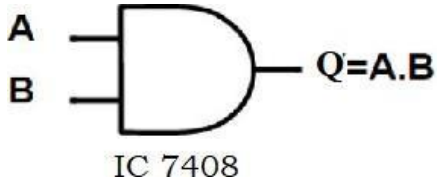
vii) Ex-NOR GATE:(IC74266)

The output is low when anyone of the inputs is high. The output is high when both the inputs are low and both the inputs are high.

SYMBOL, PIN DIAGRAMS &TRUTHTABLE:

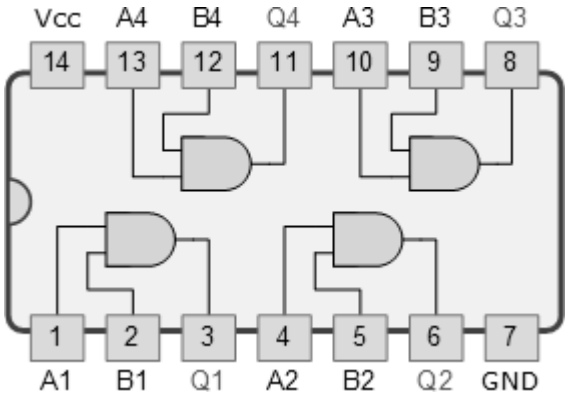
i) AND GATE

SYMBOL:



IC 7408

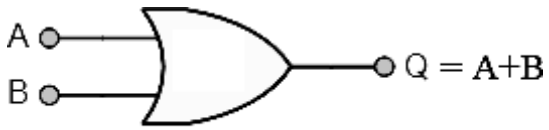
PIN DIAGRAM:



TRUTH TABLE:

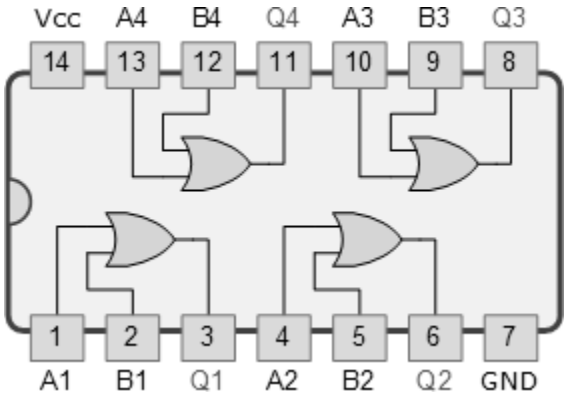
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

ii) OR GATE
SYMBOL



IC 7432

PIN DIAGRAM:

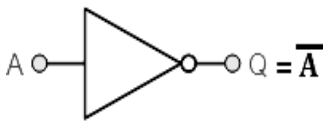


TRUTH TABLE:

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

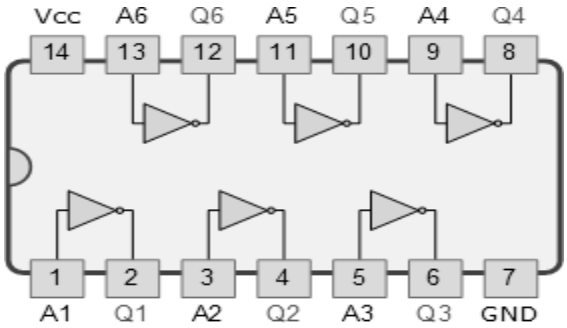
iii) NOT GATE

SYMBOL



IC 7404

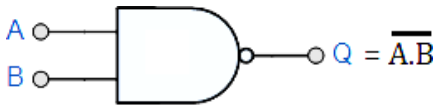
PIN DIAGRAM:



TRUTH TABLE:

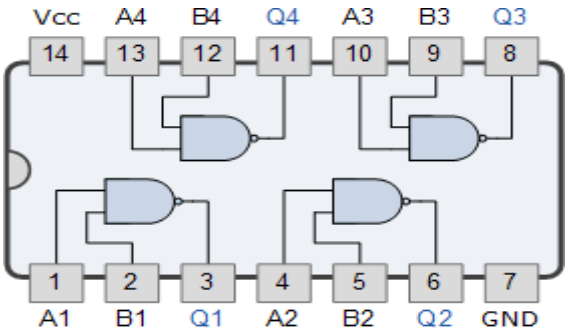
A	$\overline{A}$
0	1
1	0

iv) NAND GATE SYMBOL:



IC 7400

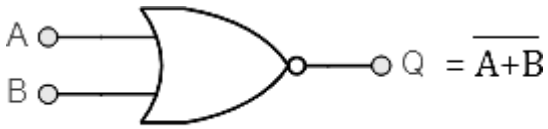
PIN DIAGRAM:



TRUTH TABLE:

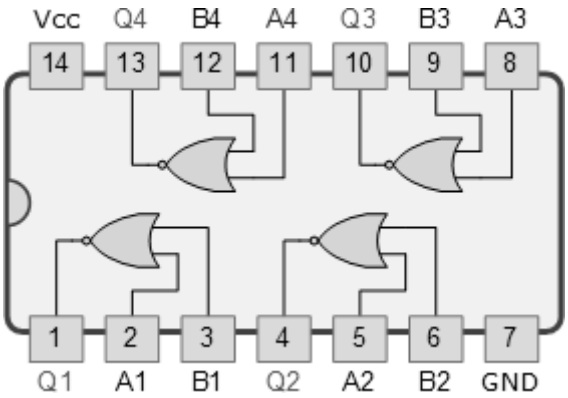
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

v) NOR GATE:



IC 7402

PIN DIAGRAM:

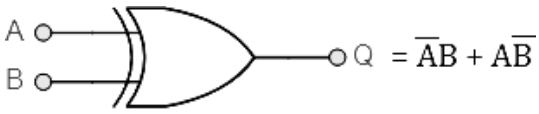


TRUTH TABLE:

A	B	$\overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0

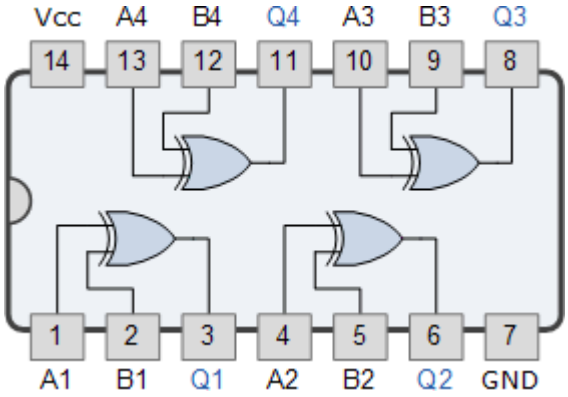
vi) EX-OR GATE

SYMBOL:



IC 7486

PIN DIAGRAM:

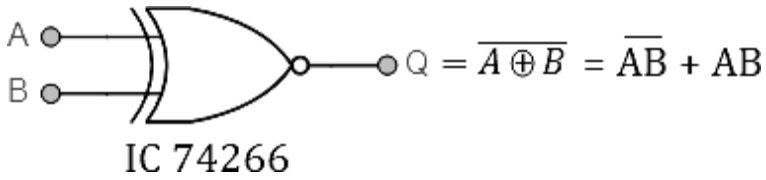


TRUTHTABLE:

A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

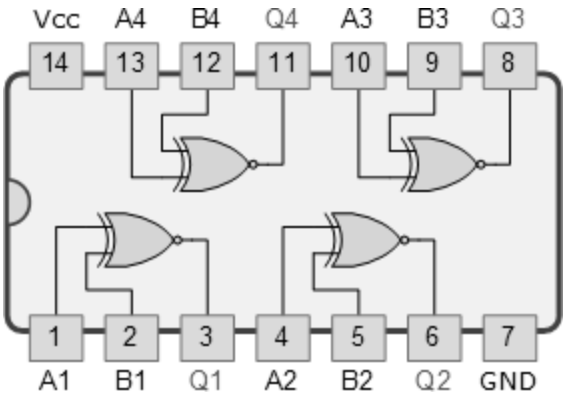
vii) EX-NOR

GATE:SYMBOL



IC 74266

PIN DIAGRAM OF IC 74266:



TRUTH TABLE:

A	B	Q =A⊙B
0	0	1
0	1	0
1	0	0
1	1	1

PROCEDURE:

1. Connect as per pin diagrams (7^{th}pin GROUND&14^{th}pin Vcc=5V).
2. Connect the input to5Vmean logic‘1’and connect the input to Ground line mean Logic ‘0’.
3. To observe any output, the output pin to be connect with resistance1kohm and LED in series and to be grounded.
4. Give the Logical inputs and observe the output& verify the truth table.

Precautions:

- All connections should be made neat and tight.
- ICs should be handled with care.
- While making connections main voltage should be kept switched off..
- When disassembling a circuit, first remove the source of power.

RESULT:

Thus the truth tables of all basic gates are verified with IC’s.

VIVA-VOCE QUESTIONS:

Define gates?
Define IC?

Give example of Demorgan’s theorem.
Write the logical equation for AND gate
What are the applications of Logic Gates?

6.Frequency response of CE amplifier

AIM:

To observe the frequency response of CE amplifier.

APPARATUS: -

S. No.	Name	Range	Quantity
1.	Transistor	BC 107	1
2.	Resistor	1kΩ,33kΩ,3.3kΩ	4,1,1
3.	Capacitor	10μF, 100μF	2, 1
4.	Function Generator	(0-3)MHz	1
5.	CRO	30MHz	1
6.	Regulated power supply	(0-30)V	1
7.	Bread Board		1
8.	Connecting wires		

Theory:

At low

circuit. So, the circuit becomes resistive at mid frequencies and the voltage gain remains constant during this range.

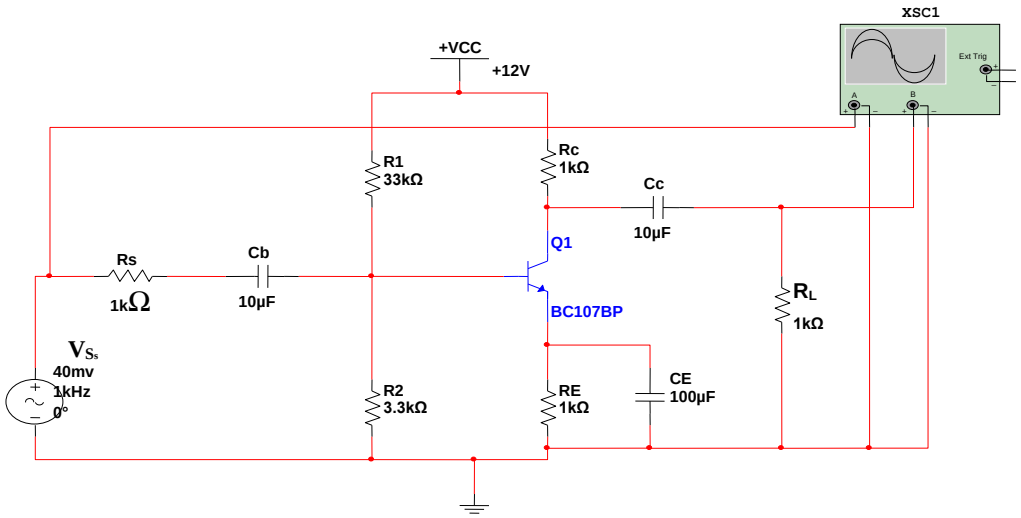
The gain is more stable in common emitter amplifier without bypass capacitor compare to with bypass capacitor. frequencies the reactance of coupling capacitor C_C is quite high and hence very small part of signal will pass through f Frequency response of an amplifier is defined as the variation of gain with respective frequency. The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at lower cut-off frequency and remains constant till higher cut-off frequency and then it falls again as the frequency increases.
rom one stage to the next stage.

At high frequencies the reactance of inter electrode capacitance is very small and behaves as a short circuit. This increases the loading effect on next stage and service to reduce the voltage gain due to these reasons the voltage gain drops at high frequencies.

At mid frequencies the effect of coupling capacitors is negligible and acts like short circuit, whereas inter electrode capacitors acts like open

CIRCUIT DIAGRAM:-

With emitter bypass capacitor Ce



PROCEDURE:

1. Connect the circuit on bread board as shown in the circuit diagram.
2. By keeping the amplitude of the input signal constant vary the frequency from 0 to 1MHZ.
3. Note down the amplitude of the output signal for corresponding values of input frequencies.
4. Calculate the voltage gain in decibels.
5. Plot in semi-log graph between gain versus frequency and calculate the band width.

OBSERVATIONS:

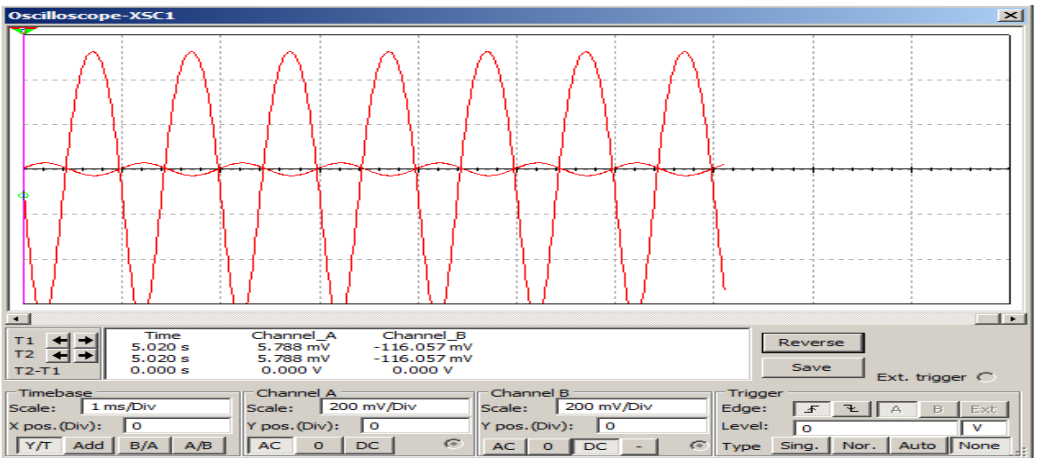
Input Voltage V_{IN} = -----

S.NO	FREQUENCY	V_{OUT}	GAIN(Av) = V_{OUT}/V_{IN}	GAIN in dB=20log Av

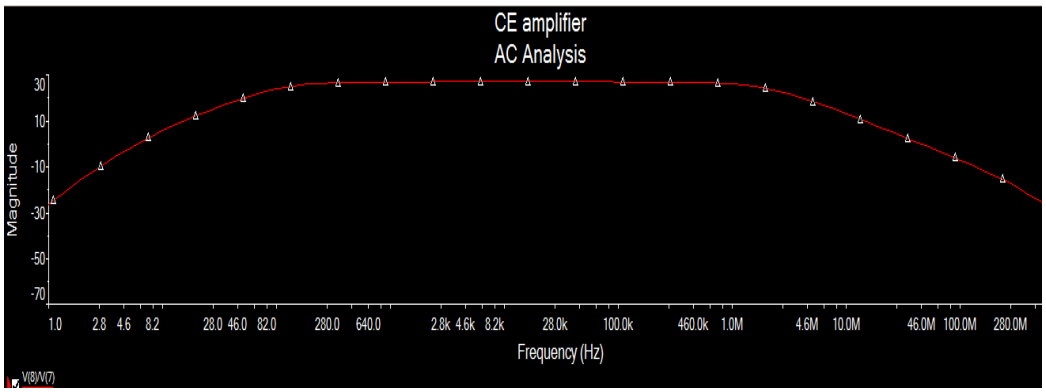
CALCULATIONS:

i. Determine lower cut-off frequency and upper cut-off frequency from the graph.
ii. Calculate Band width.

Expected waveforms:



GRAPH:



PRECAUTIONS:

1. Test Transistors before assembling the circuits
2. Resistors should be connected properly without interchanging the values.
3. Check the continuity of the connecting wires.

APPLICATIONS:

1. Audio amplifiers
2. Radio Transmitters and Receivers.

RESULT:

i. Lower cut-off frequency =
ii. Upper cut-off frequency =
iii. Band width =

7.Design of two stage RC Coupled amplifier.

Aim: To plot the frequency response characteristics of two stages RC coupled amplifier and calculate the bandwidth.

Apparatus Required:

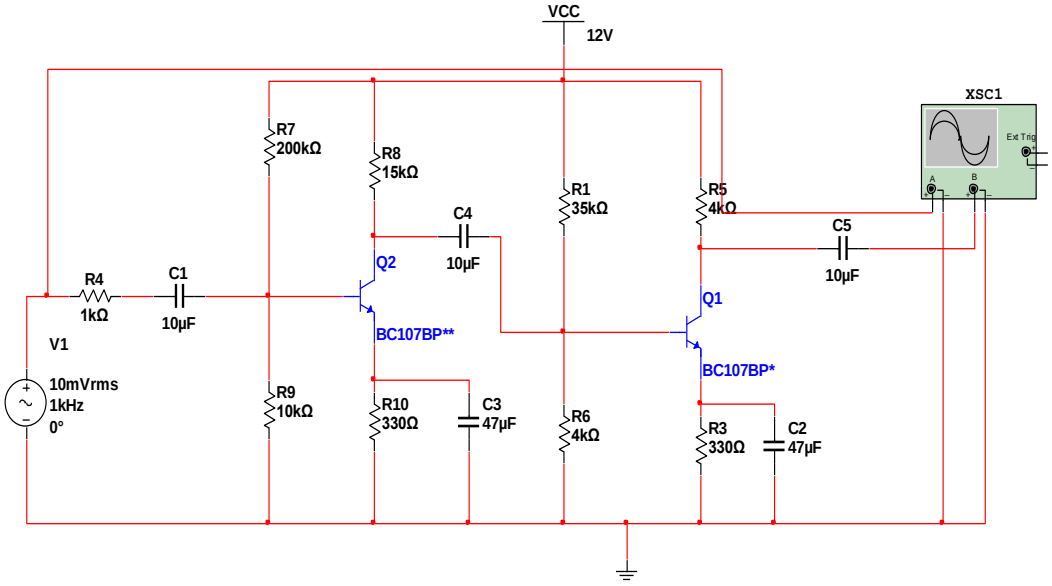
S. No.	Name	Range	Quantity
1.	Transistor	BC 107	2
2.	Resistor	330Ω, 4kΩ,1kΩ,200kΩ,10kΩ,35kΩ,15kΩ	2,2,1,1,1, 1,1,
3.	Capacitor	10µF, 47 µF	3,2
4.	Function Generator	(0-3)MHz	1
5.	CRO	30MHz	1
6.	Regulated power supply	(0-30)V	1
7.	Bread Board		1
8.	Connecting wires		

Theory:

To improve gain characteristics of an amplifier, two stages of CE amplifier can be cascaded. While cascading, the output of one stage is connected to the input of another stage. If R and C elements are used for coupling, that circuit is named as RC coupled amplifier.

Each stage of the cascade amplifier should be biased at its designed level. It isPossible to design a multistage cascade in which each stage is separately biased and coupled to the adjacent stage using blocking or coupling capacitors. In this circuit each of the two capacitors C1 & C2 isolate the separate bias network by acting as open circuits to dc and allow only signals of sufficient high frequency to pass through cascade.

Circuit diagram:



PROCEDURE:

1. Connect the circuit on bread board as shown in the circuit diagram.
2. By keeping the amplitude of the input signal constant, vary the frequency from zero to 1 MHz.
3. Note down the amplitude of the output signal for corresponding values of input frequencies.
4. Calculate the voltage gain in decibels.
5. Plot in semi-log graph between gain versus frequency and calculate the band width.

OBSERVATIONS:

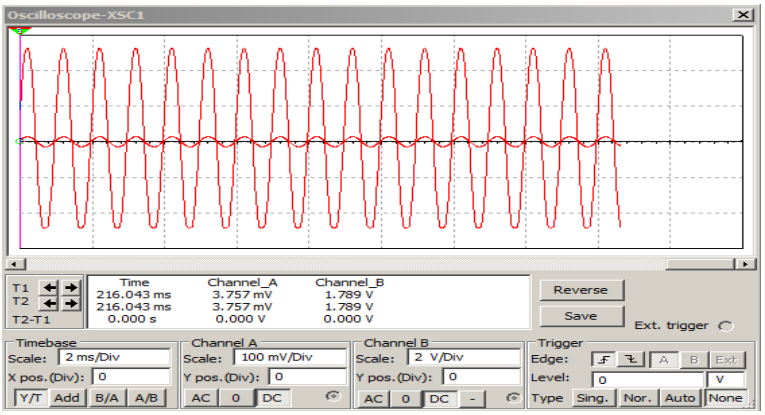
Input voltage V_{IN} = -----

S.NO	FREQUENCY	V_{OUT}	GAIN(Av) = V_{OUT}/V_{IN}	GAIN in dB=20log Av

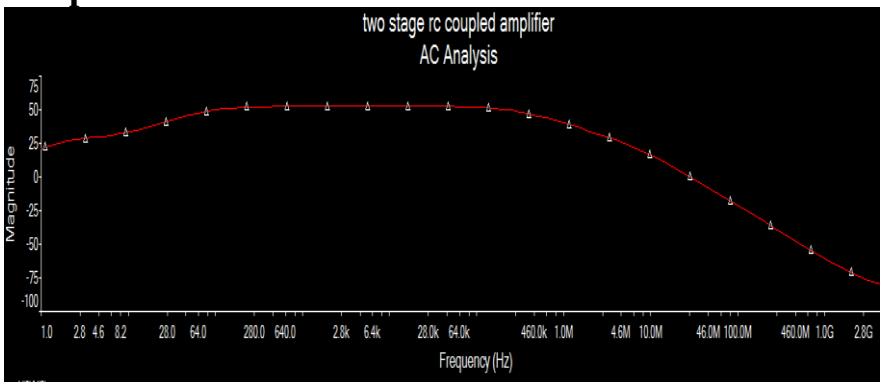
CALCULATIONS:

i. Determine lower cut-off frequency and upper cut-off frequency from the graph.
ii. Calculate Band width.

Expected wave forms:



Graph:



PRECAUTIONS:

1. Test Transistors before assembling the circuits

2. Resistors should be connected properly without interchanging the values.

3 .Check the continuity of the connecting wires.

APPLICATIONS:

To get the desired gain.

RESULT:

i. Lower cut-off frequency =
ii. Upper cut-off frequency =
iii. Band width =

Viva Questions:-

1. What is the necessity of cascading?
2. Define 3-dB bandwidth.
3. Why RC-coupling is preferred in audio range?
4. Explain various types of coupling.
5. What is loading effect?
6. What is meant by RC coupling?
7. What is importance of cascade coupling?
8. What is Darlington pair?

Verification of Truth Tables of S-R, J-K & D flip flops using respective ICs

Aim :

To verify the truth tables of R-S, J-K and D flip-flops using respective IC (Integrated Circuit)s.

Apparatus :

i) IC 7400, IC 7476, IC 7474
ii) LEDs
iii) Breadboard
iv) Connecting wires
v) Regulated Power Supply

Theory :

A Flip-flop is a 1-bit edge-triggered storage device. It is another name for bistable multivibrator. A flip-flop is one of the most versatile building blocks of digital computer systems. The output of a flip-flop changes its state when driven by a trigger (edge) pulse. It can be used as a memory cell since it holds the information until the arrival of the next trigger pulse at the input. Different types of flip-flops include R-S flip-flop, J-K flip-flop, and D - flip-flop.

R-S Flip-flop

The R-S flip-flop is used to temporarily hold or store information until it is needed. The S and R inputs control the state of the flip-flop when the clock pulse goes from LOW to HIGH. The flip-flop will not change until the clock pulse is on a rising edge. When both S and R are simultaneously HIGH, it is uncertain whether the outputs will be HIGH or LOW.

J-K Flip-flop

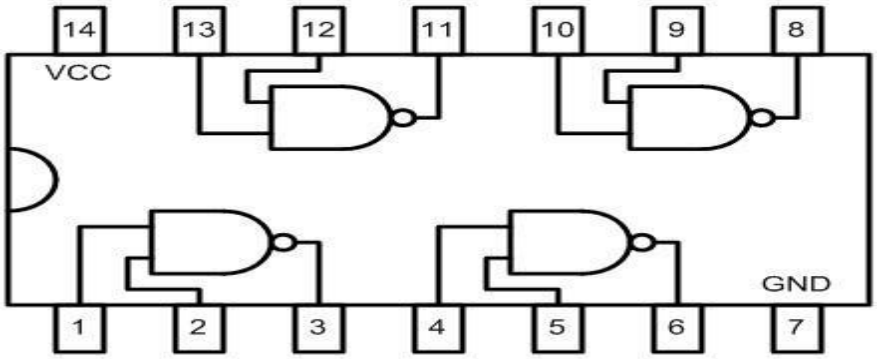
The JK Flip-Flop is a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”.

D Flip-flop

A D (or Delay) Flip-Flop is a digital electronic circuit used to delay the change of state of its output signal (Q) until the next rising edge of a clock timing input signal occurs.When the clock signal is low, the flip-flop holds its current state and ignores the D input. When the clock signal is high, the flip-flop samples and stores D input. The value that was previously fed into the D input is reflected at the flip-flop's Q output.

Circuit Diagrams:

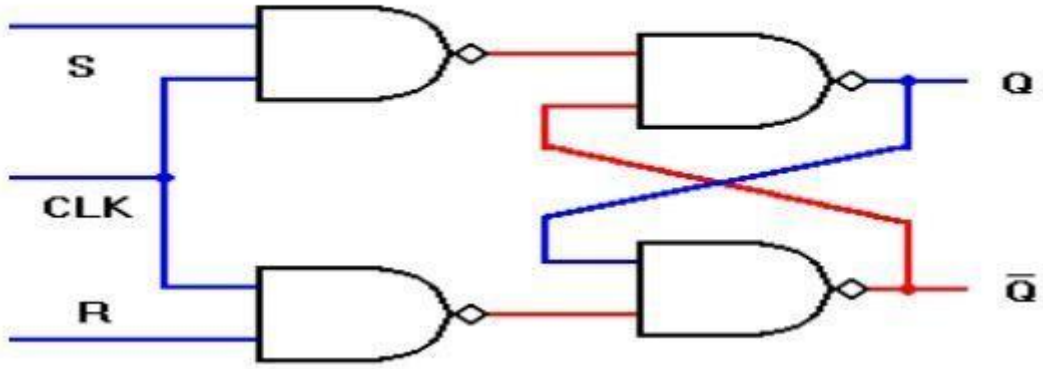
R-S Flip-flop



7400 Quad 2 Input NAND

Pin Diagram of IC 7400

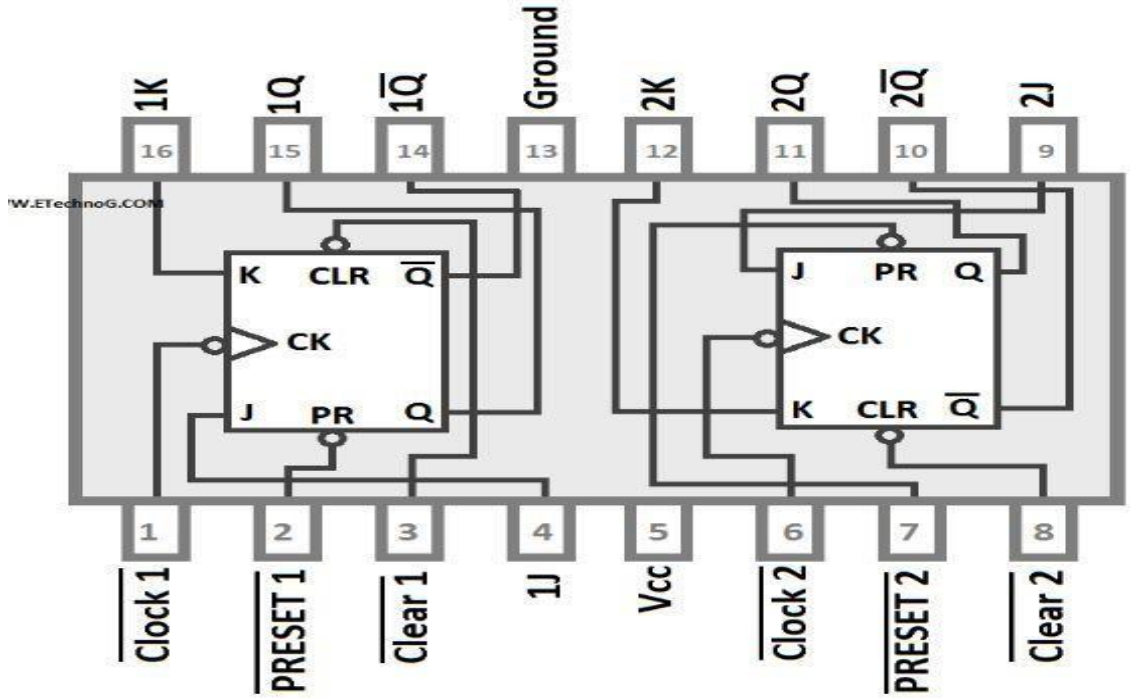
Clocked RS- Flip-flop using NAND gates



Clocked RS- Flip-flop Truth Table

Inputs			Output	State
CLK	S	R	Q	
X	0	0	No Change	Previous
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	-	Forbidden

J-K Flip-flop



Pin Diagram of IC 7476

Truth Table

Input					Output	
Preset	Clear	Clock	J	K	Q	Q'
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	↓	0	0	No change	
1	1	↓	0	1	0	1
1	1	↓	1	0	1	0
1	1	↓	1	1	Toggle	

D – Flip-flop

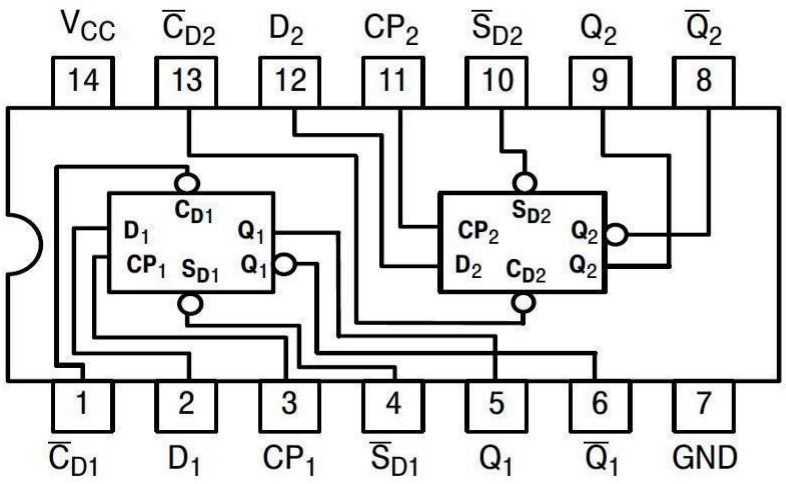


Fig : Pin diagram of IC 7474

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{PR}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	X	X
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q_0	$\overline{Q}_0$

Procedure:

1. Insert the corresponding IC on the breadboard.
2. Identify the pins and make necessary connections as per the circuit diagram.
3. The logical inputs are applied for all the possible combinations.
4. Connect LEDs to Q and Q' of corresponding IC in order to verify the states of flip-flops.

Precautions:

- All connections should be made neat and tight.
- ICs should be handled with care.
- Switch off the power supply while making connections.
- When disassembling a circuit, first remove the source of power

Result:

Hence the truth tables of R-S, J-K and D flip-flops have been verified using respectiveICs.